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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/259,849

03/01/1999

PAUL A. FARRAR

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07/30/2004

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EXAMINER

PERALTA, GINETTE

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/259,849

Applicant(s)

FARRAR, PAUL A.

Examiner

Ginette Peralta

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-77 and 186-189 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-77 and 186-189 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-17, 19-25, 27-32, 34-36, 38--44, 50-77, and 186-189 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann et al. (U. S. Pat. 6,358,849 B1) in view of Brown et al. (U. S. Pat. 6,168,704 B1)

Regarding claim 1, Havemann et al. discloses a method of forming a conductor that comprises depositing an insulator 122 over a planarized surface 120; etching a trench having a depth on the insulator 122; depositing a barrier layer 150 on the insulator; depositing a seed layer 152 directly on the barrier layer; depositing a conductor on the seed area by a deposition process.

Havemann et al. discloses the claimed invention with the exception of removing the barrier layer and seed layer from selected areas of the insulator, and depositing the conductor by a selective deposition process after removing the barrier layer and the seed layer.

Brown et al. discloses a method of forming a conductor that comprises etching a trench having a depth on an insulator; depositing a barrier layer 400A on the insulator; depositing a seed layer 400B directly on the barrier layer; removing the barrier layer and seed layer from selected areas of the insulator, leaving a seed area; and depositing a conductor on the seed area by a selective deposition process after removing the barrier layer and seed layer from selected areas of the insulator, wherein a seed area is formed by the removal of the barrier and seed layers, and the conductor is selectively deposited for the disclosed intended purpose of reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier layer and the seed layer from selected areas and to deposit the conductor by a selective deposition process only in those areas left after the removal of the barrier layer and the seed layer in the invention of Havemann et al. for the disclosed intended purpose of Brown et al. of reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents.

Regarding claim 2, Havemann et al. discloses depositing the barrier layer 150 by physical vapor deposition.

Regarding claim 3, Havemann et al. discloses etching the trench to a depth about equal to the depth of the insulator.

Regarding claim 4, Havemann et al. discloses a method of forming a conductor that comprises depositing an oxide layer 122 over a planarized surface 120; etching a trench on the oxide layer 122; depositing a barrier layer 150 on the oxide layer; depositing a seed layer 152 on the barrier layer without a layer between the seed layer and the barrier layer; depositing a conductor on the seed area by a deposition process.

Havemann et al. discloses the claimed invention with the exception of removing the barrier layer and seed layer from selected areas of the oxide layer, and depositing the conductor after removing the barrier layer and the seed layer.

Brown et al. discloses a method of forming a conductor that comprises etching a trench having a depth on an insulator; depositing a barrier layer 400A on the insulator; depositing a seed layer 400B directly on the barrier layer; removing the barrier layer and seed layer from selected areas of the insulator, leaving a seed area; and depositing a conductor on the seed area by a selective deposition process after removing the barrier layer and seed layer from selected areas of the insulator, wherein a seed area is formed by the removal of the barrier and seed layers, and the conductor is selectively deposited for the disclosed intended purpose of reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the barrier layer and the seed layer from selected areas and to deposit the conductor by a selective deposition process only in those areas left after the removal of the barrier layer and the seed layer in the invention of Havemann et al. for the disclosed intended purpose of Brown et al. of reducing the manufacturing cost, reducing consumption of electroplating solution and CMP consumables, reducing the amount of post-metallization deposition CMP needed and reducing the amount of hazardous effluents.

Regarding claim 5, Havemann et al. discloses that the oxide layer comprises a silicon dioxide.

Regarding claim 6, Havemann et al. discloses that the oxide layer is a fluorinated silicon oxide layer (col. 3, ll. 14-16).

Regarding claim 7, Havemann et al. discloses that the seed layer is deposited on the barrier layer by physical vapor deposition.

Claims 8-17, 19-25, 27-32, 34-36, 38-44, 50-77, and 185-189, recite the same steps as claims 1 and 4, however, with specific material limitations imposed on the layers recited, as specifically addressed in the following:

- Regarding the limitation that the insulator layer is made of a polymer, Havemann et al. discloses that as an alternative to fluorinated silicon dioxide, the dielectric layer can be made of organic polymers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a

polymer instead of the fluorinated silicon oxide, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

- Regarding the limitation that the insulator layer is made of oxide is disclosed by Havemann et al..
- Regarding claim 10, it is well known to one of ordinary skill in the art that polymer (claim 8), polyimide (claim 9) and foamed polymer (claim 10) are equally good as interlayer dielectric (ILD). Therefore, substituting polyimide in Havemann's insulator layer 122 of Fig. 1 with foamed polymer is not an act of invention, and hence, unpatentable. *In re Ruff*, 256 F.2d 590, 118 USPQ 340, 343 (CCPA 1958). Unpatentability not only applies where equivalency is disclosed in the prior art, but also where such equivalency would have been obvious. *Id.* at 599, 118 LISPQ at 348. It would have been obvious to one ordinarily skilled in the art at the time the invention was made to select any one of these materials as a suitable insulator layer of Havemann's, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability (e.g., if low-k dielectric is desired) for the intended use as a matter of design choice. *In re Leshin*, 125 LISPQ 416.
- Regarding the limitation that the barrier layer is made of tantalum or tantalum nitride is disclosed by Havemann et al.. Furthermore, Havemann et al. discloses

that layer 152 is a copper seed layer formed directly on the tantalum nitride barrier layer.

- Regarding the limitation that the barrier layer is titanium is disclosed by Havemann et al..
- Regarding the limitation that the seed layer is made of copper is disclosed by Havemann et al..
- Regarding the limitation that the seed layer is made of gold or silver, is well-known in the art.
- Regarding the limitation that the conductive layer is made of gold, silver or aluminum, is well-known in the art.
- Regarding the limitation that the barrier layer and/or seed layer is deposited either by the PVD or CVD method is well-known in the art, as recited by Havemann et al..
- Regarding the limitation that the Al conductive layer is deposited on the seed layer by CVD is conventional, and hence well-known in the art.
- Regarding the limitation that the Al conductive layer is deposited to an amount sufficient to fill the trench is obvious as this shows that it is well known and desirable in the art of forming a plug or interconnect.
- Regarding the limitation that the copper seed layer is deposited to a depth of approximately five-hundred angstroms thick, or to five-hundred angstrom

below the top of the trench is trivial, since if it is deposited more than the specified amount, it is no longer a seed layer, but a conductive layer.

Furthermore, Havemann et al. discloses that the copper seed layer is 10 nm thick.

- Regarding the limitation that the TaN barrier layer is deposited above the conductor to a depth of approximately five-hundred angstroms is an obvious matter of design choice within skill in the art that would not yield any unexpected results.
- Regarding the limitation that the barrier layer is deposited to a depth of between fifty angstroms and one thousand angstroms is well known to one of ordinary skill in the art. It would have been an obvious matter of design choice to vary the size of the barrier layer, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

3. Claims 18, 26, 33 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann et al. in view of Brown et al. as applied to claims 1-17, 19-25, 27-32, 34-36, 38--44, 50-77, and 185-189 above, and further in view of Ting et al..

Havemann et al. as modified by Brown et al. discloses the claimed invention with the exception of the seed layer being formed of aluminum-copper, and the conductor being gold, silver or aluminum and being deposited by electroless plating.

Ting et al. discloses a method of forming a conductor that comprises a seed layer of aluminum-copper, the step of depositing copper on the seed layer that comprises depositing aluminum on the seed area by selective CVD, wherein the aluminum-copper layer is used as an alternative to a copper layer, and furthermore Ting et al. discloses that copper, gold, silver and aluminum are alternative materials for forming conductors. It would have been obvious to one having ordinary skill in the art at the time the invention was made to an aluminum-copper seed layer instead of a copper seed layer and to form a conductor comprising any of gold, silver, aluminum or copper, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Response to Arguments

4. Applicant's arguments filed 11/17/03 have been fully considered but they are not persuasive.

With regards to applicant's argument that Havemann is not a valid reference since it's filing date is 12/21/99, and that this date is after applicant's priority claim, it is noted that the effective filing date of Havemann corresponds to that of provisional application 60/114039, and furthermore it is noted that the subject matter relied upon in Havemann is supported by the provisional application. It is further submitted that if the application properly claims benefit under 35 U.S.C. 119(e) to a provisional application, the effective filing date is the filing date of the provisional application for any claims

which are fully supported under the first paragraph of 35 U.S.C. 112 by the provisional application. MPEP 706.02. Therefore the Havemann patent is still applicable as prior art under 35 U.S.C. 102 (e) and the rejection still stands.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814